WHAT IS CLAIMED IS:

1. A non-volatile memory device comprising:

a semiconductor substrate including a cell region and a peripheral circuit region;

a plurality of active regions disposed in the cell region;

a plurality of cell line patterns crossing over the active regions;

a tunnel insulating layer and floating gate electrodes interposed between the cell line patterns and the active regions;

a plurality of control gate lines, each disposed adjacent to a sidewall of the cell line patterns;

a dummy region interposed between the cell region and the peripheral circuit region; and

at least one dummy line pattern which is disposed in the dummy region;

wherein each of the cell line patterns comprises a couple of spacer lines and a source line;

wherein the couple of spacer lines are comprised of a plane sidewall and a curved sidewall; and

wherein the source line is interposed between a couple of spacer lines and electrically connected to the active region between a couple of spacer lines.

2. The non-volatile memory device according to claim 1, further comprising a liner spacer interposed between the source line and each of the spacer lines, and the floating gate electrodes, wherein the liner spacer insulates the source line and the floating gate electrodes.

3. The non-volatile memory device according to claim 1, wherein the tunnel insulating layers and the floating gate electrodes are interposed between the spacer lines and the active region, and wherein each of the control gate lines is disposed on the plane sidewall of each of the spacer lines.

4. The non-volatile memory device according to claim 1, further comprising a control gate insulating layer interposed between each of the spacer lines, the floating gate electrodes, the active region, and the control gate lines.

5. The non-volatile memory device according to claim 1, wherein the dummy region surrounds the cell region.

6. The non-volatile memory device according to claim 5, wherein the dummy line pattern forms a loop surrounding the cell region.

7. The non-volatile memory device according to claim 1, wherein the dummy line pattern comprises:

a couple of dummy spacer lines which are disposed apart from each other in the dummy region, the dummy spacer lines comprising a curved sidewall and a plane sidewall; and

a dummy source line interposed between the couple of dummy spacer lines, wherein the couple of dummy spacer lines are disposed for the curved sidewalls thereof to face each other.

8. The non-volatile memory device according to claim 7, wherein each of the dummy spacer lines is made of a silicon oxide layer.

9. The non-volatile memory device according to claim 7, wherein the dummy source line is made of a doped polysilicon layer.

10. The non-volatile memory device according to claim 7, further comprising a device isolating layer disposed in the semiconductor substrate and under the dummy line pattern.

11. The non-volatile memory device according to claim 7, further comprising a dummy floating gate electrode interposed between the device isolating layer and each of the dummy spacer lines.

12. The non-volatile memory device according to claim 7, further comprising:

a dummy control gate line disposed on the plane sidewall of the dummy spacer lines; and

a dummy control gate insulating layer interposed between each of the dummy spacer lines, the semiconductor substrate, and the dummy control gate line.

13. The non-volatile memory device according to claim 1, wherein the dummy line pattern and a furthest peripheral cell line pattern in the cell region are spaced apart by a predetermined distance which is the same as the distance between the cell line patterns.

14. A method of forming a memory device comprising:

preparing a substrate having a cell region, a dummy region, and a peripheral circuit region;

forming a control gate insulating layer, a control gate conductive layer and an oxidation layer on a substrate, the substrate having a cell region, a dummy region, and a peripheral circuit region, the dummy region being interposed between the cell region and the peripheral region;

forming a plurality of cell line patterns in the cell region;

forming a plurality of dummy line patterns in the dummy region, wherein a distance between a dummy line pattern and an adjacent cell line pattern is the same as the distance between cell line patterns;

forming a control gate insulating layer, a control gate conductive layer

and an oxidation layer on the substrate; and

planarizing the control gate insulating layer and the oxidation layer by chemical mechanical processing.